What is claimed is:

1. A method for performing power distribution analysis for I/O circuits in an integrated circuit (IC) design, said I/O circuits having defined placement locations within a power distribution network of said design, comprising the steps of:

a) calculating maximum and average currents for each of said I/O circuits, and an average logic current demand per node;

b) creating a resistance model of said power distribution network comprising nodes and resistors corresponding to points on buses of said network and resistivities corresponding to said points;

c) indexing each of said I/O circuit currents and said average logic current demand per node to the node in said model closest to the corresponding I/O circuit location;

d) solving the resistance and current source model resulting from step (c) for voltages at the nodes; and

e) outputting the results.

2. The method of claim 1, further comprising:

(f) comparing said results against specified voltage drop (IR) and electromigration (EM) limits of said design to identify violations of said limits; and

(g) changing said I/O circuit placement locations to correct said violations.

3. The method of claim 2, further comprising

repeating steps (a) - (g) until step (f) does not identify any violations.

4. The method of claim 1, wherein said design utilizes an area-array type I/O circuit distribution.

5. The method of claim 1, wherein said design utilizes a peripheral type I/O circuit distribution.

6. The method of claim 1, wherein step (d) uses a sparse matrix solver.

7. A method comprising:

establishing a distribution of I/O circuits in a power distribution network of an IC design;

generating a resistance model comprising resistivities at nodes corresponding to said network;

relating currents of said I/O circuits and an average logic current demand per node to nodes in said resistance model;

solving for voltages at said nodes in terms of said resistivities, I/O circuit currents and average logic current demand per node;

identifying ones of said voltages not in compliance with IR and EM limits of said design; and

re-arranging said distribution to bring said identified voltages into compliance.

8. The method of claim 7, further comprising adjusting a granularity of said resistance model for a desired accuracy of said model.

9. The method of claim 7, further comprising using lumped resistance values to represent routing layers of said design in said model.

10. The method of claim 7, wherein said solving step comprises:

formulating a conductance matrix from said resistance model and a current matrix from said I/O circuit currents and average logic current demand per node;

calculating voltages at said nodes using relationships between said conductance matrix and said current matrix established by said relating step.

11. The method of claim 7, wherein said identifying step comprises:

comparing said voltages against a design rule specifying an allowable variation of said voltages as a percentage of a supply voltage.

12. The method of claim 7, wherein said step of generating a resistance model comprises:

repeating a bus pattern by a repeat factor, said bus pattern including a bus starting location, a bus width and a bus end.

13. A computer-usable medium storing computer-executable instructions, said instructions when executed implementing a process comprising:

from a power distribution network for an IC design, generating a resistance model comprising resistivities at nodes corresponding to said network;

relating currents of I/O circuits connected to said network, and an average logic current demand per node, to nodes in said resistance model;

solving for voltages at said nodes in terms of said resistivities, I/O circuit currents and average logic current demand per node; and

outputting the results, said results identifying ones of said voltages not in compliance with IR and EM limits of said design.

14. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps of performing power distribution analysis for I/O circuits in an integrated circuit (IC) design, said I/O circuits having defined placement locations within a power distribution network of said design, comprising the steps of:

a) calculating maximum and average currents for each of said I/O circuits, and an average logic current demand per node;

b) creating a resistance model of said power distribution network comprising nodes and resistors corresponding to points on buses of said network and resistivities corresponding to said points;

c) indexing each of said I/O circuit currents and said average logic current demand per node to the node in said model closest to the corresponding I/O circuit location;

d) solving the resistance and current source model resulting from step (c) for voltages at the nodes; and

e) outputting the results.

15. A computer system comprising:

a memory containing computer-executable instructions;

a processor coupled to said memory for executing said instructions, said instructions when executed performing a process comprising:

from a power distribution network for an IC design, generating a resistance model comprising resistivities at nodes corresponding to said network;

relating currents of I/O circuits connected to said network, and an average logic current demand per node, to nodes in said resistance model;

solving for voltages at said nodes in terms of said resistivities, I/O circuit currents and average logic current demand per node; and

outputting the results, said results identifying ones of said voltages not in compliance with IR and EM limits of said design.